

Fig. 2

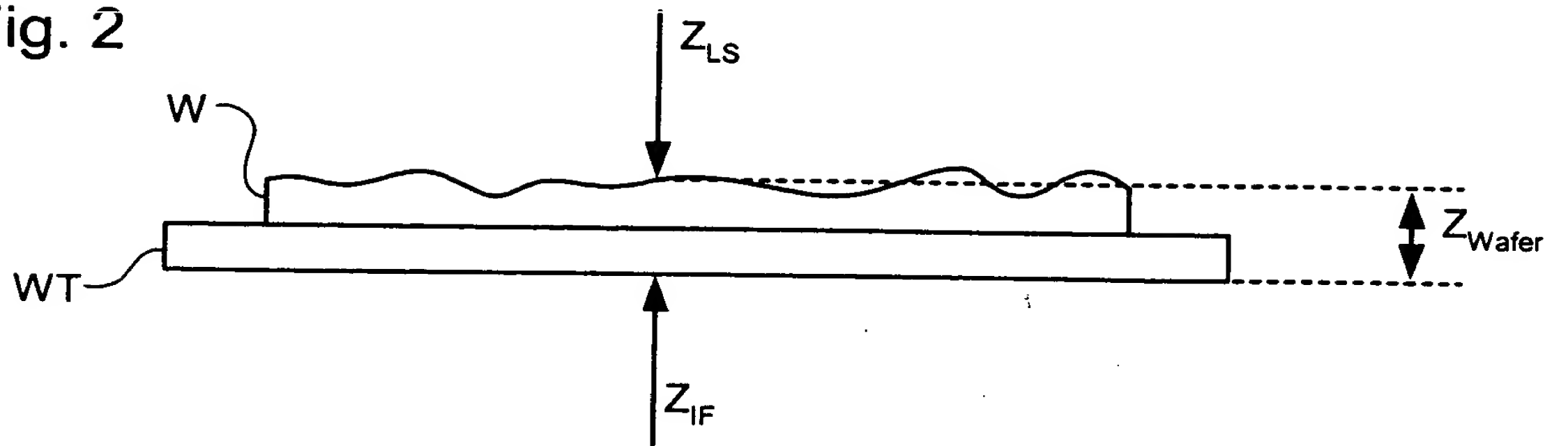


Fig. 3

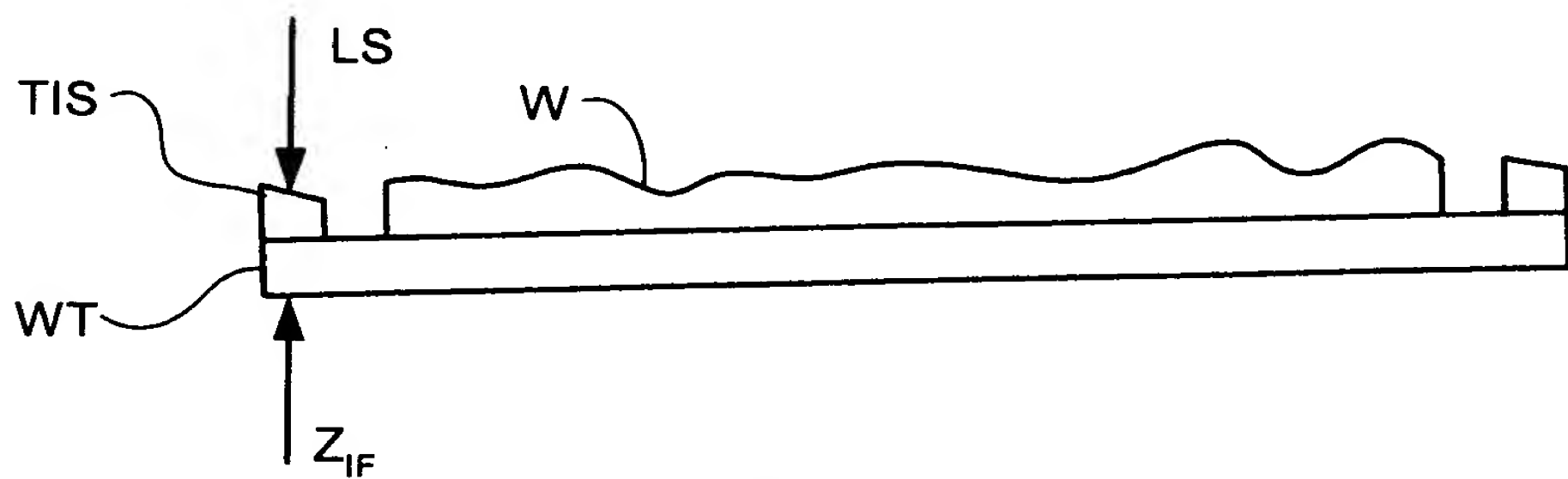


Fig. 4

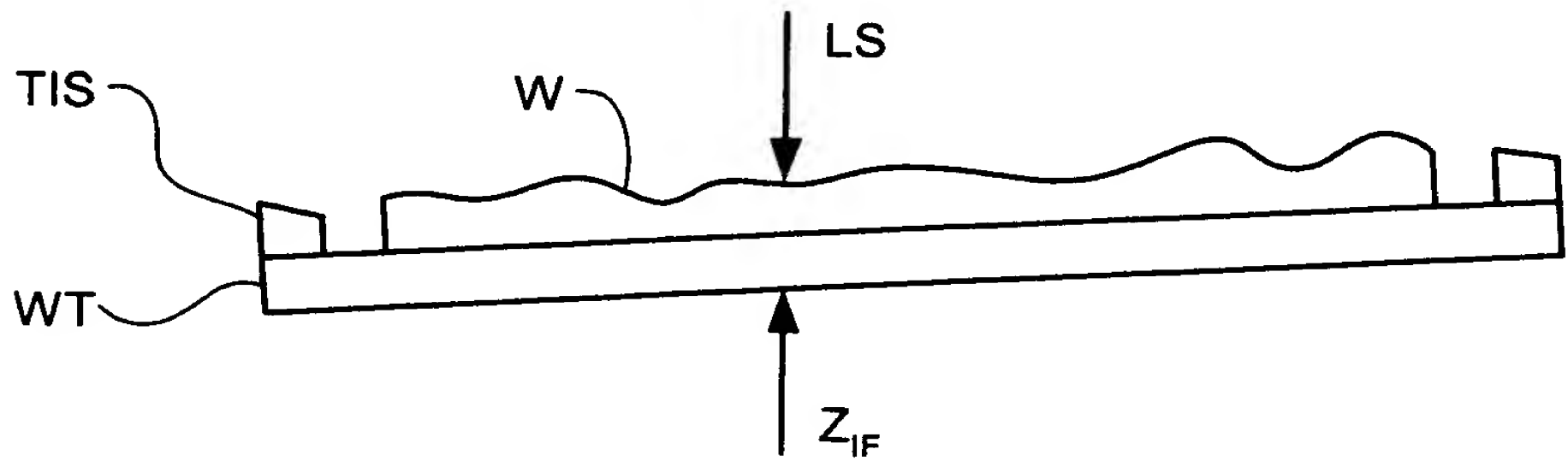


Fig. 5

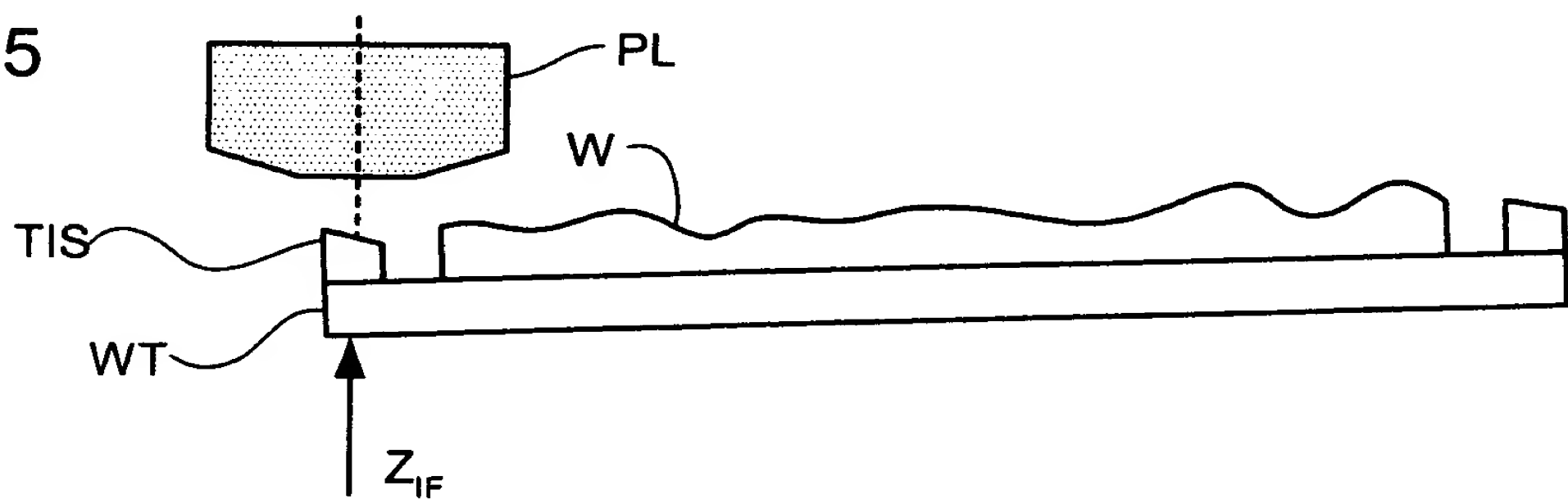


Fig. 6

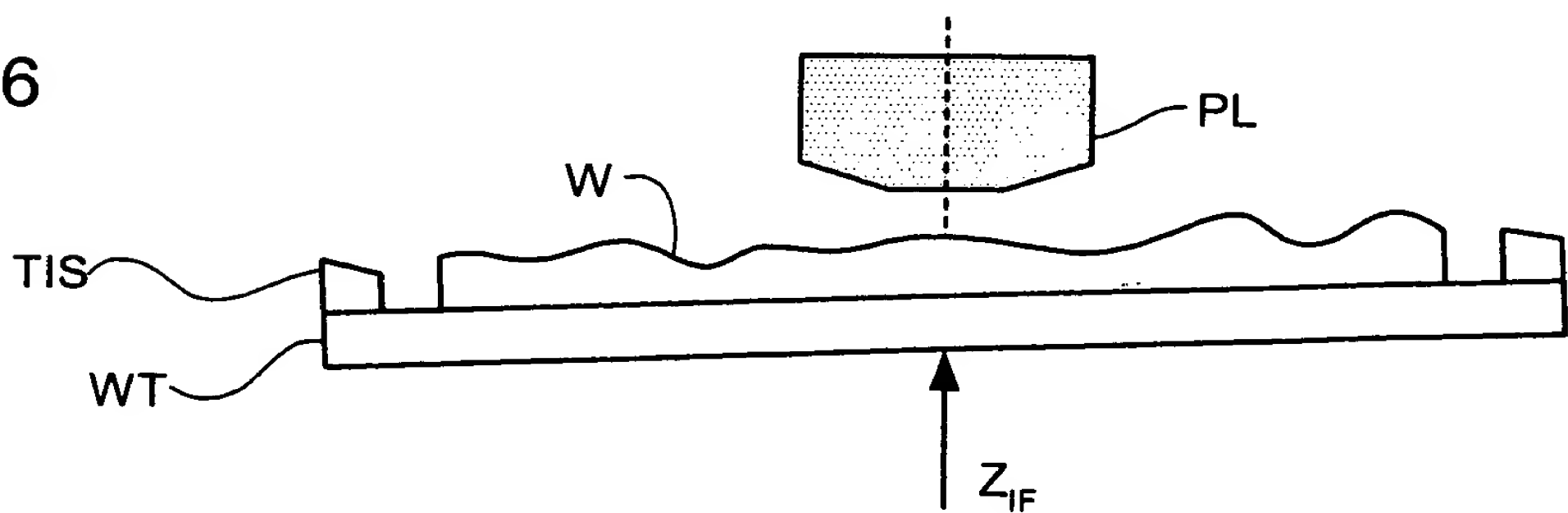


Fig. 7

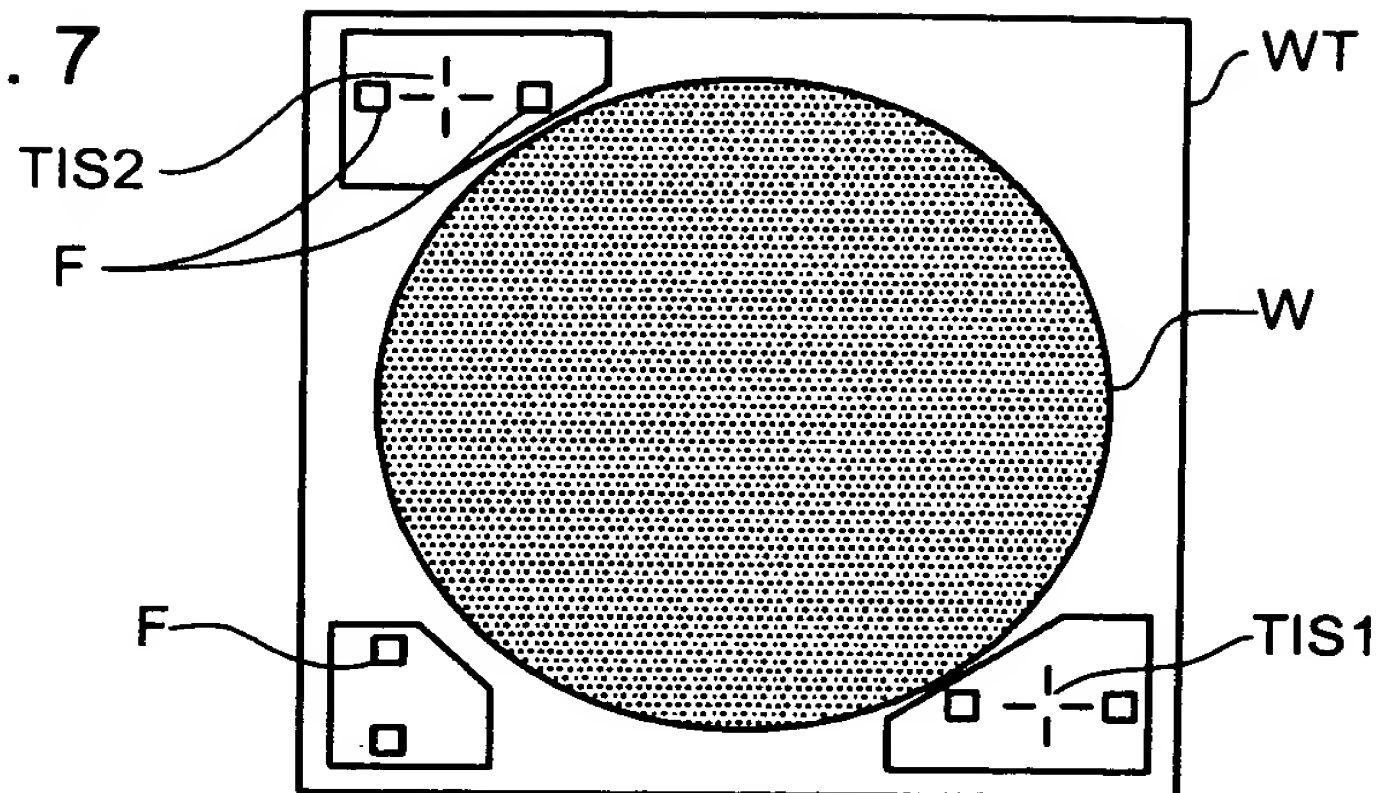


Fig. 9

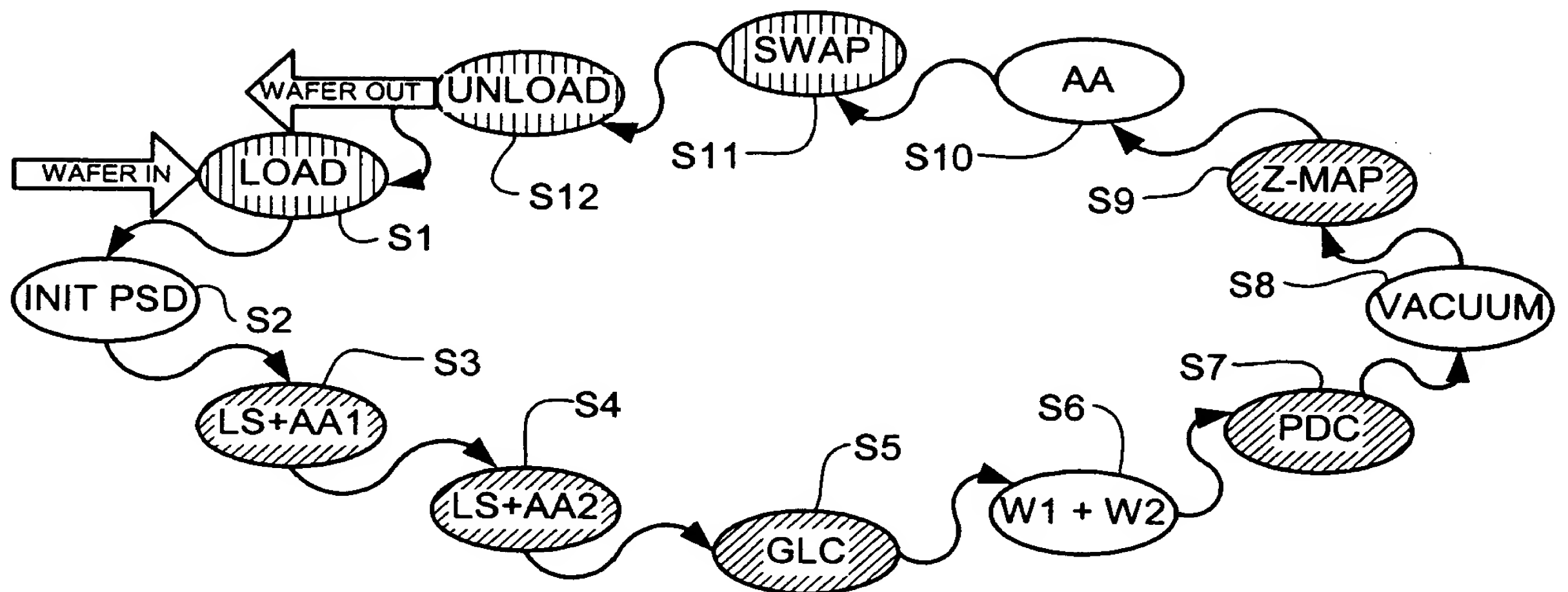


FIG. 10

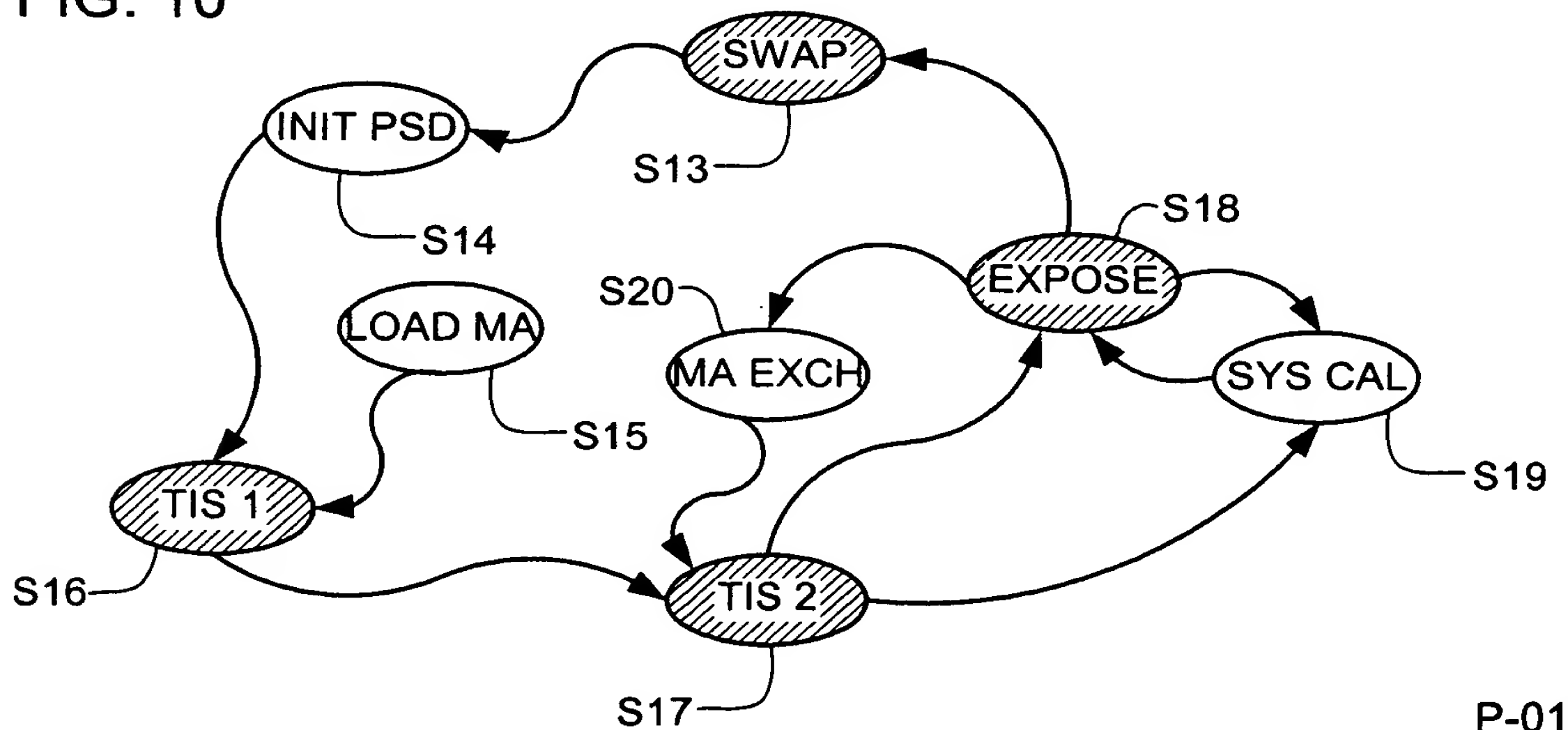


Fig. 8

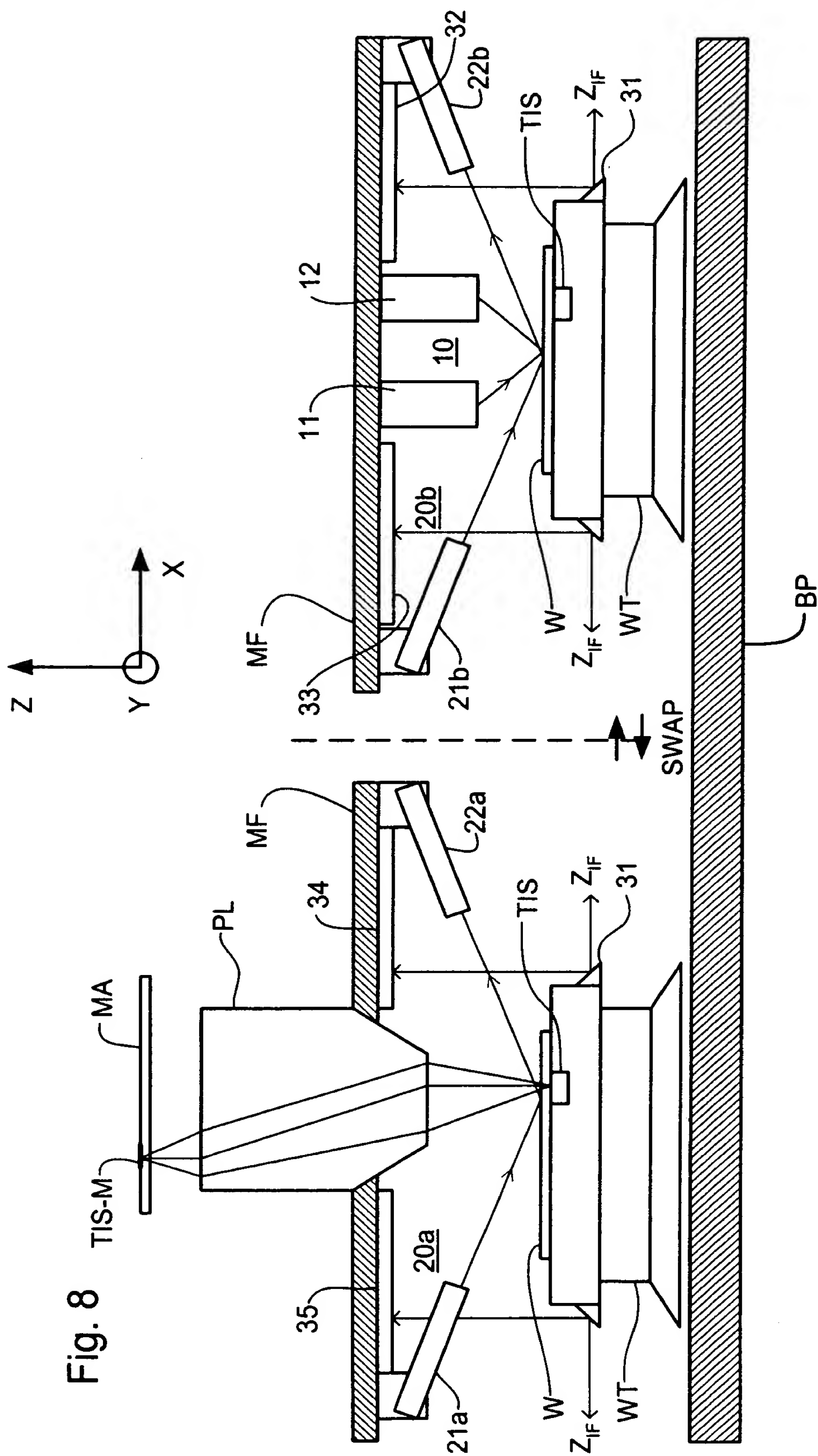


Fig. 11

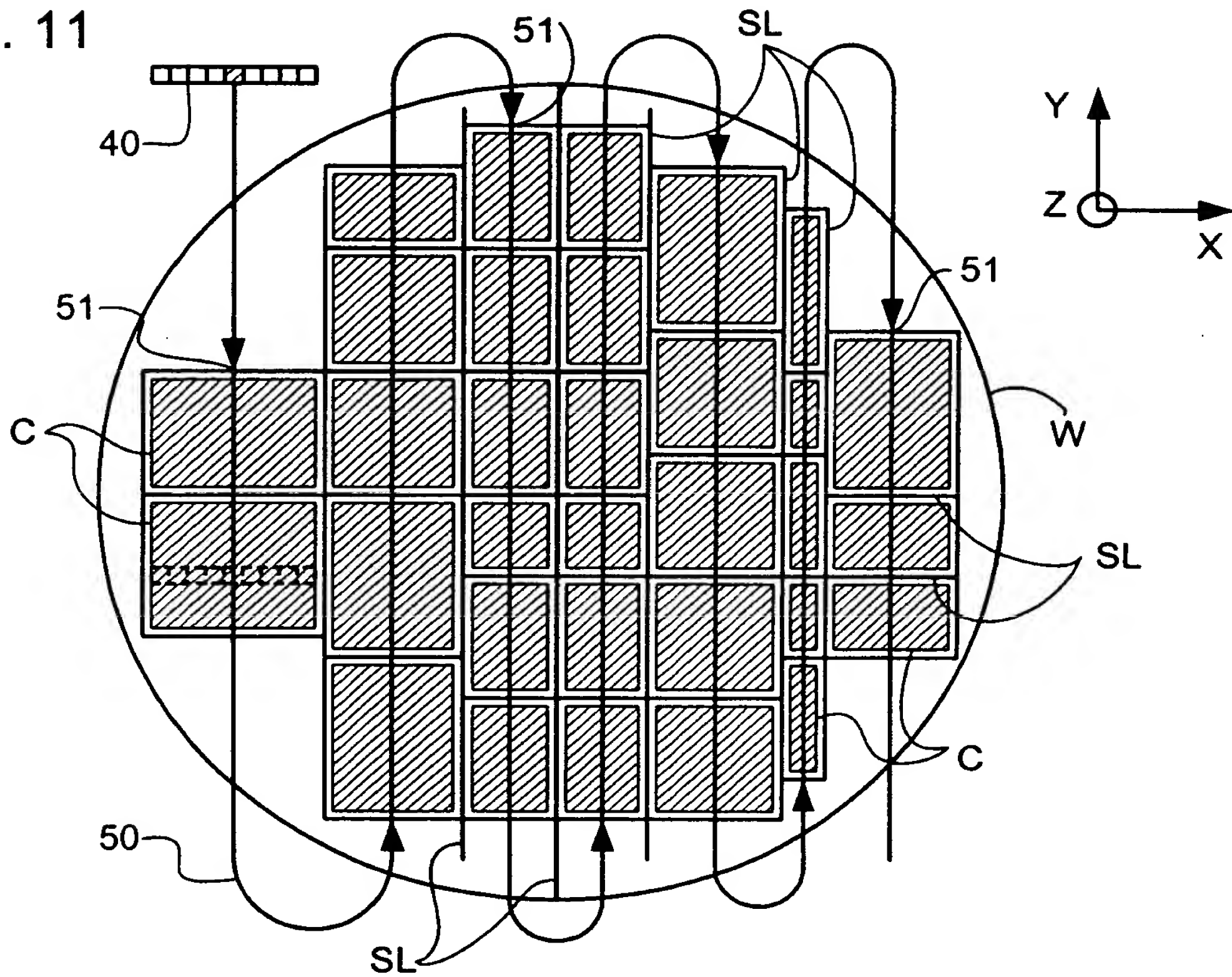


Fig. 12

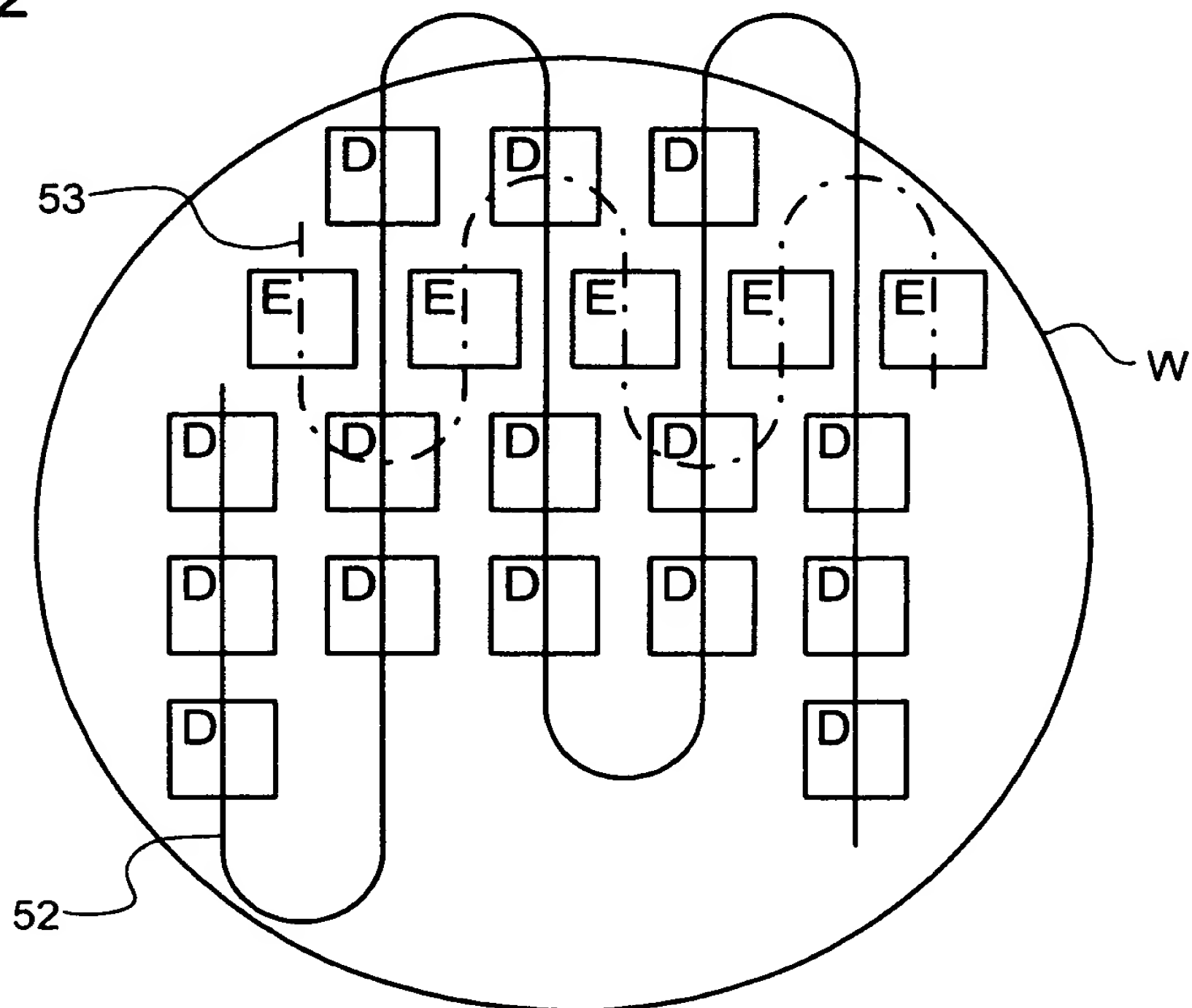


Fig. 13

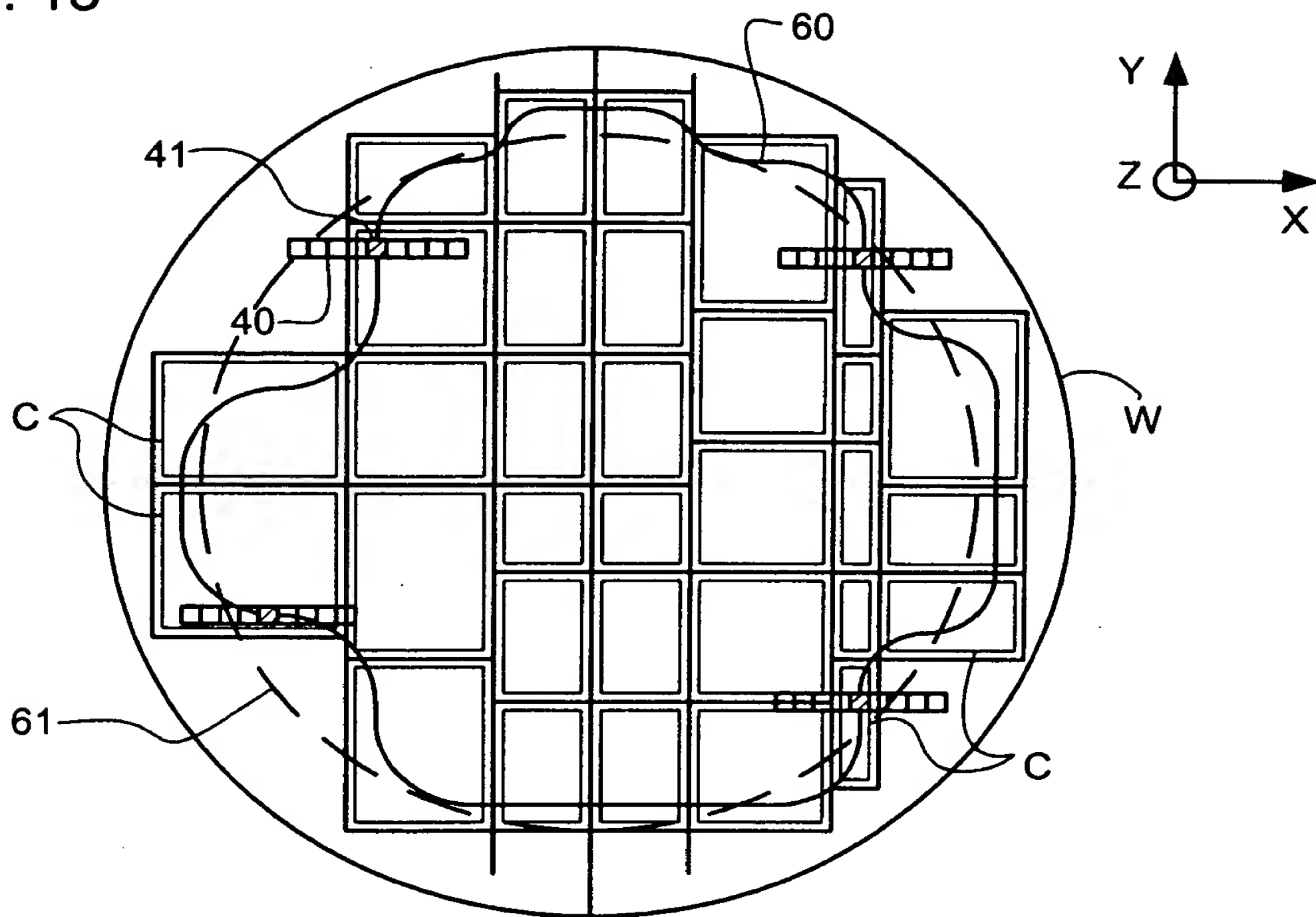


Fig. 15

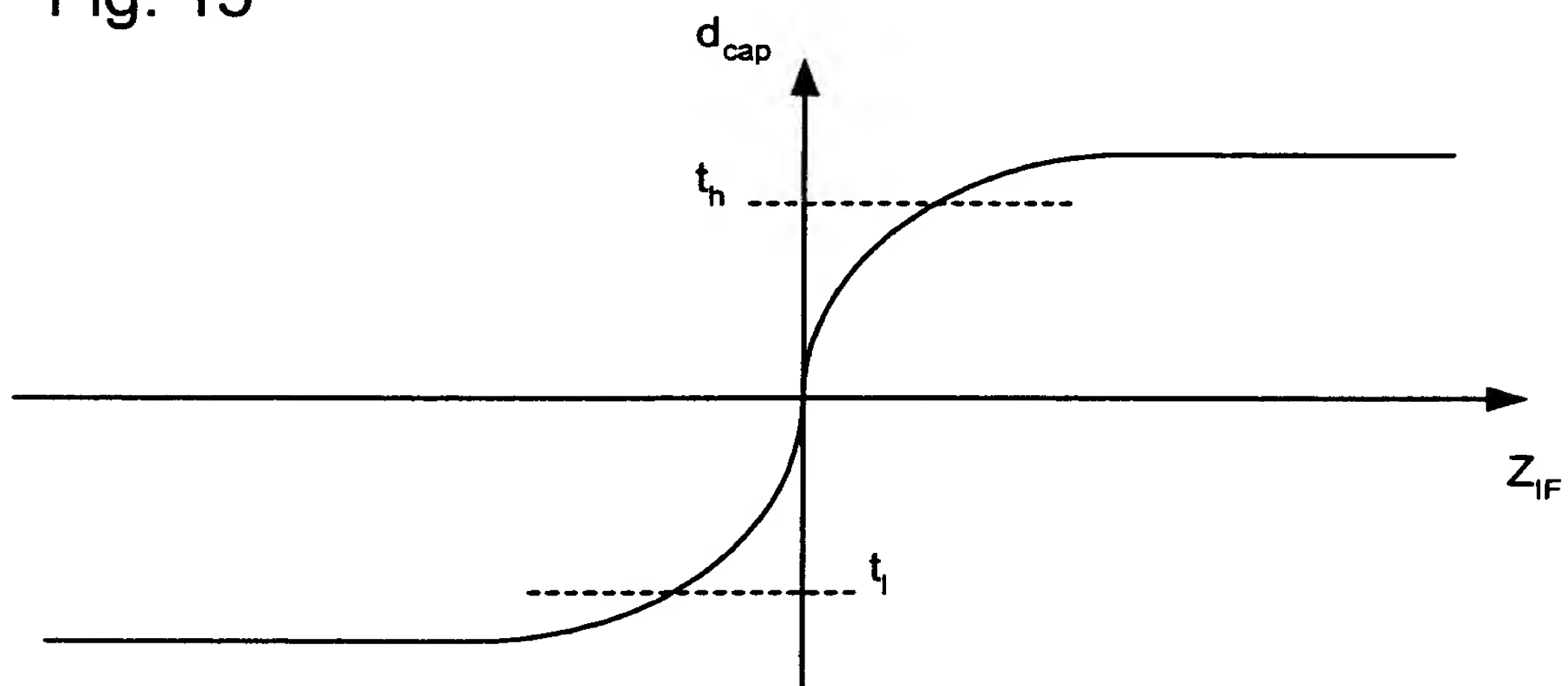
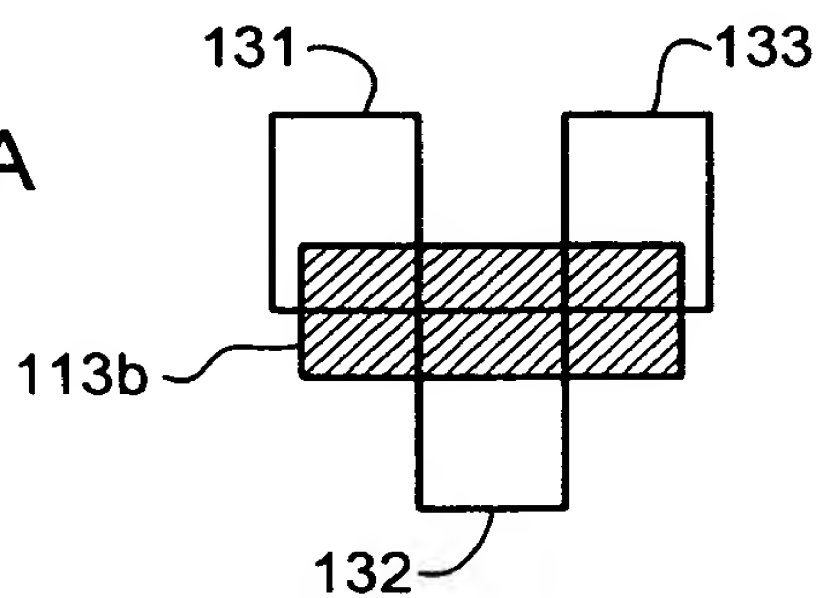
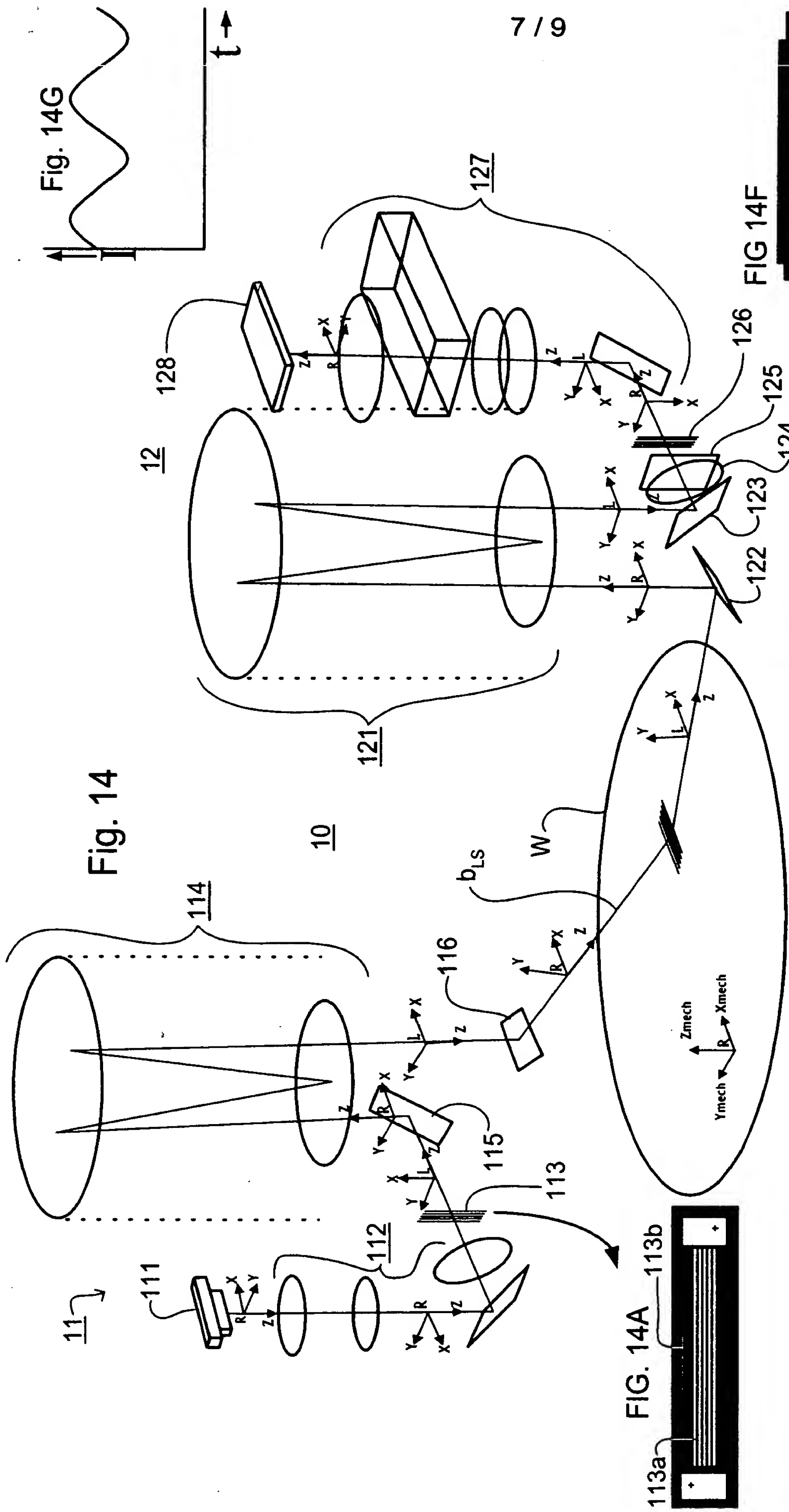


Fig. 15A





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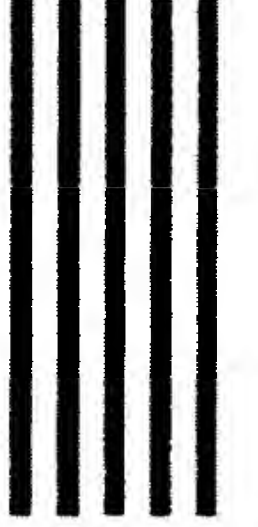
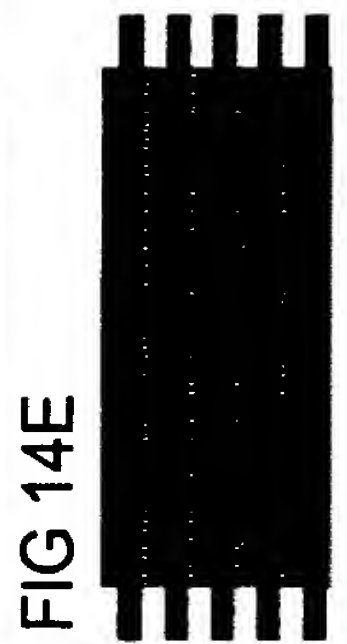
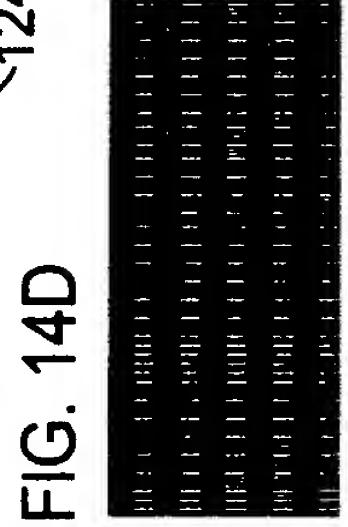
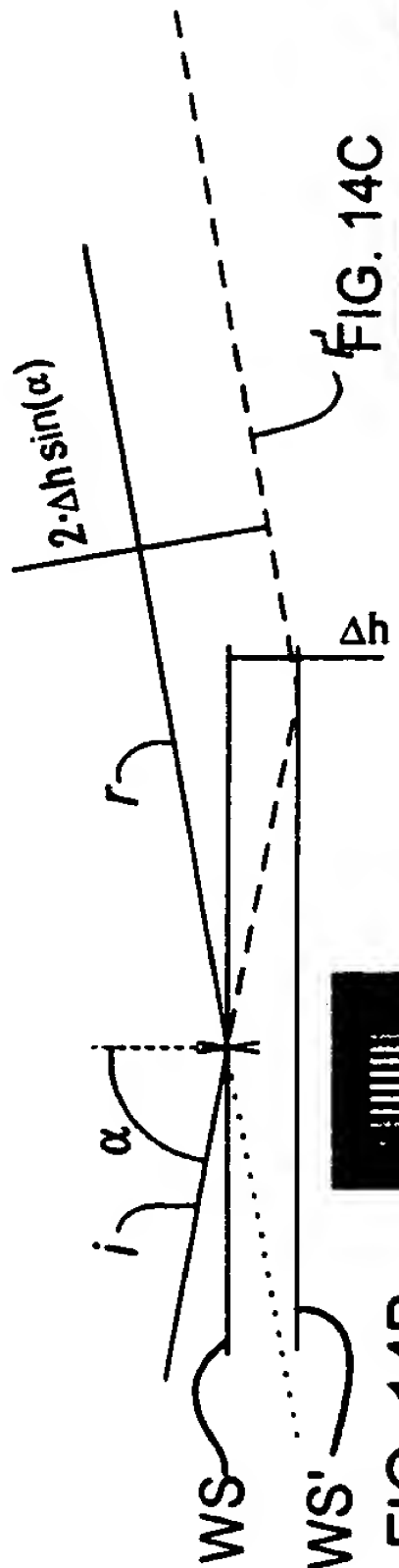
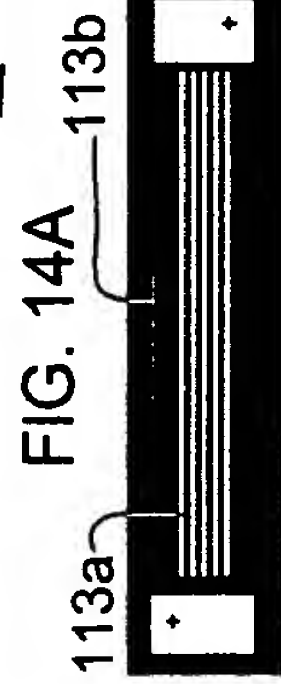


FIG. 14F

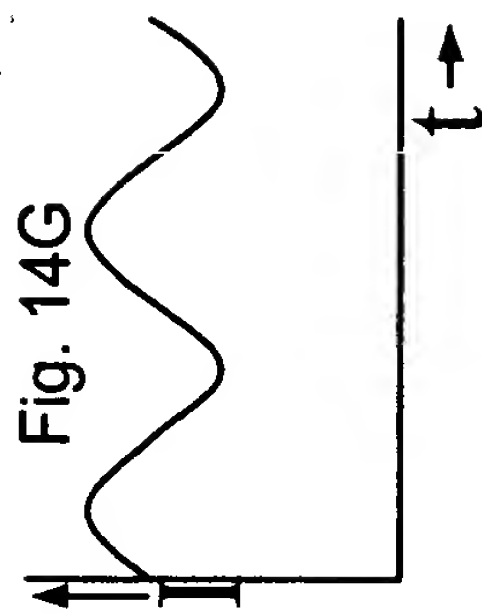
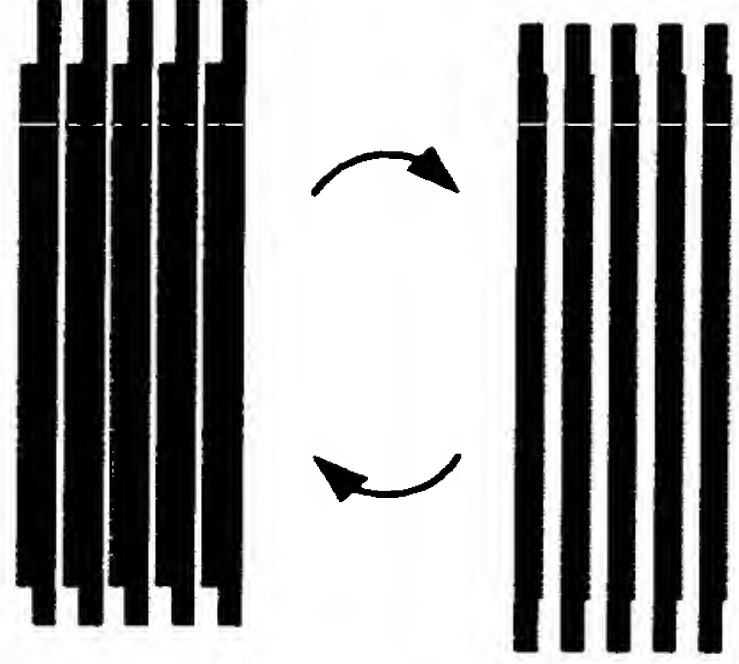


Fig. 16

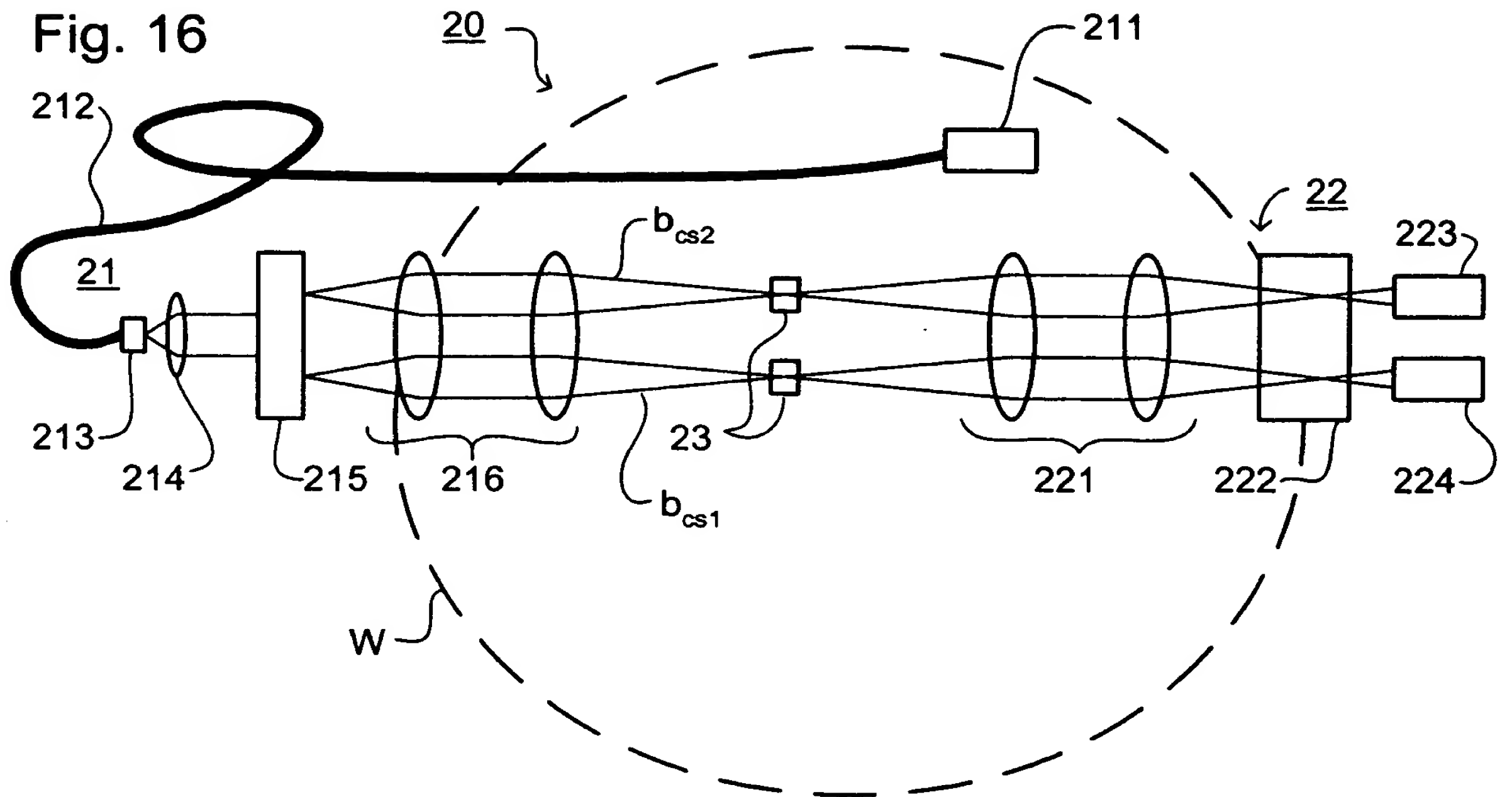


Fig. 17

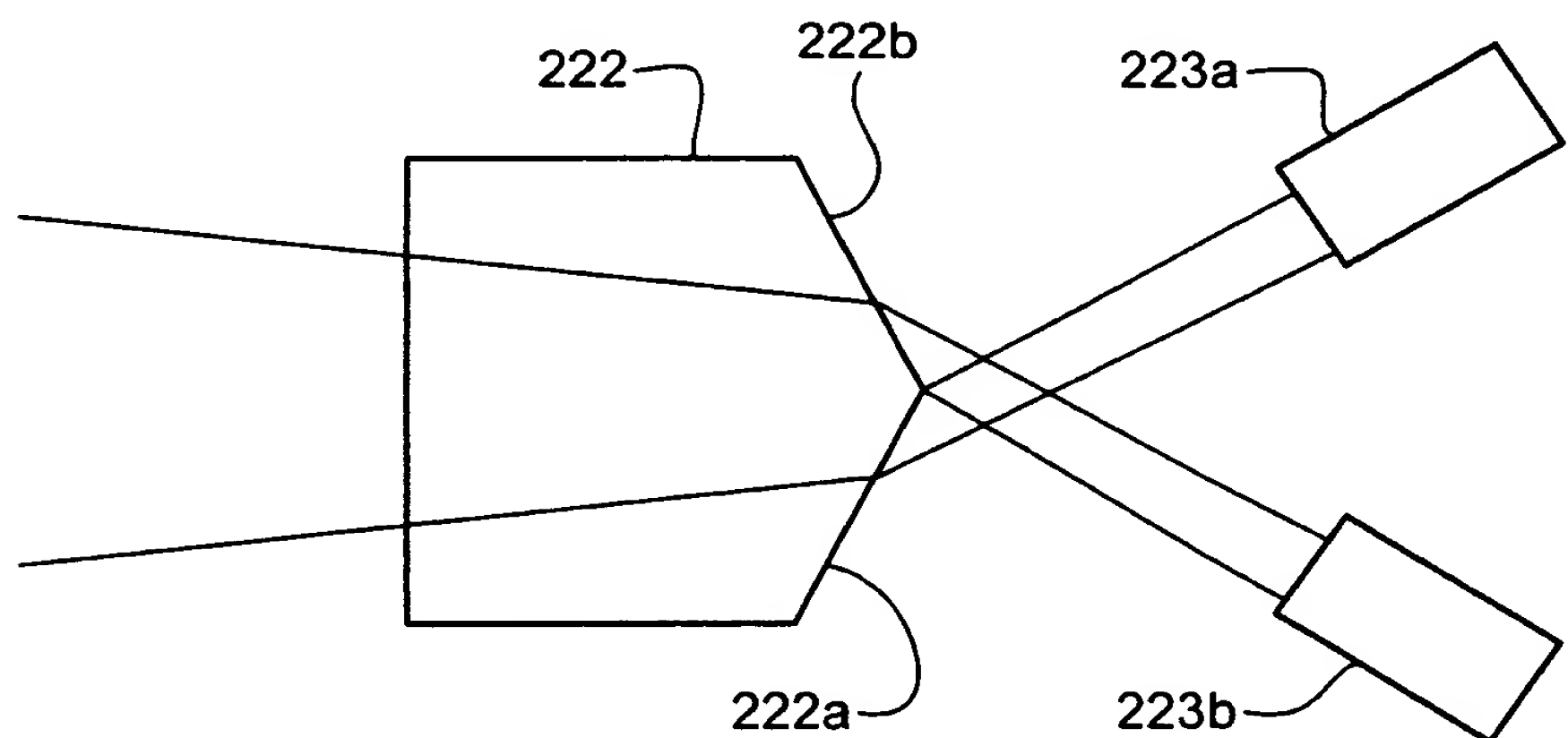


Fig. 18

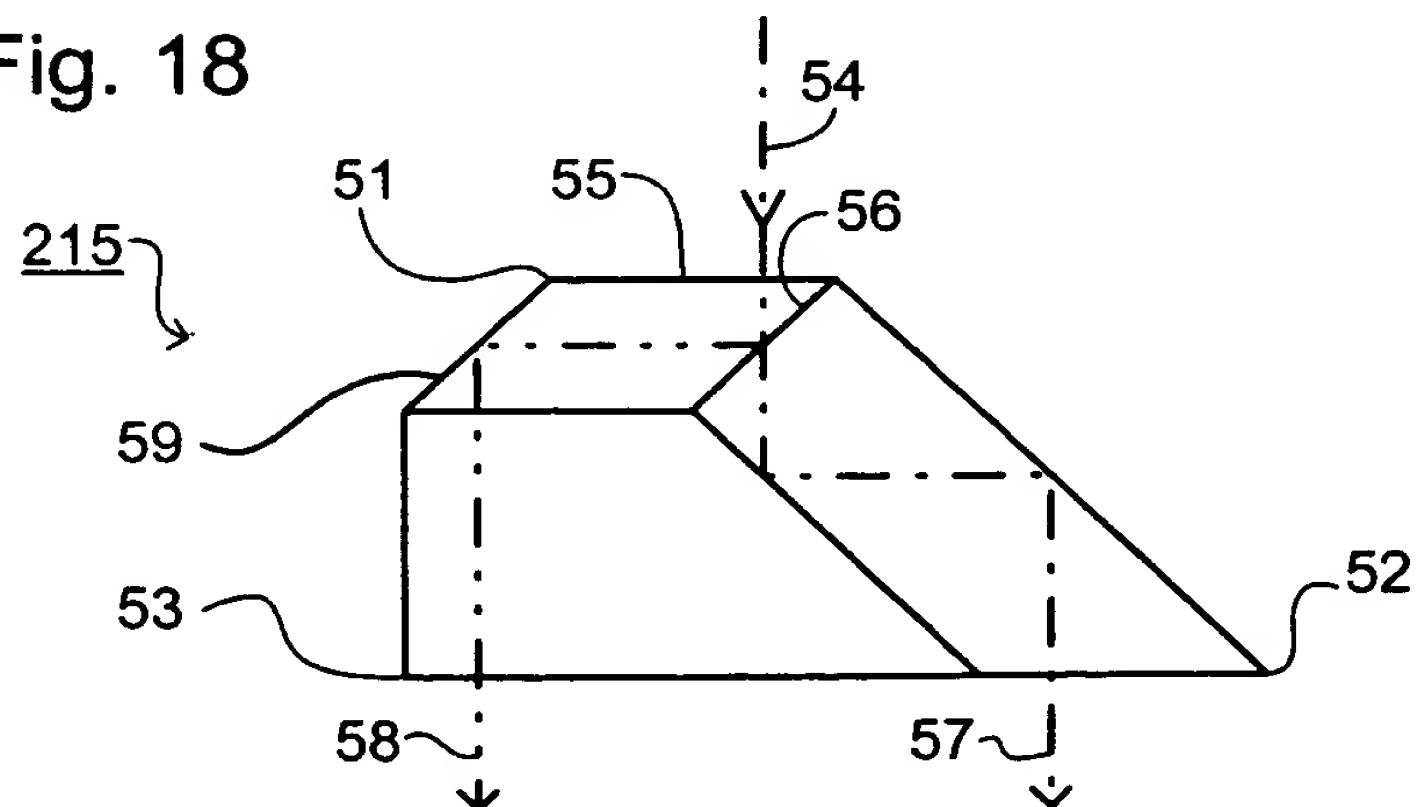


Fig. 19

A schematic diagram of a wafer assembly. A solid rectangular block represents the wafer, with a dashed line below it indicating a reference plane. A thin layer, labeled WT , is on top of the wafer. Above this layer is a wavy surface, labeled W . A vertical arrow labeled Z_{LS} points down to the wavy surface. A vertical arrow labeled Z_{IF} points up to the bottom of the wafer. A horizontal double-headed arrow labeled δX indicates a lateral displacement. A vertical double-headed arrow labeled δW_{LS} indicates a vertical displacement of the wavy surface. A vertical double-headed arrow labeled Z_{Wafer} indicates the thickness of the wafer. A dashed line represents the original flat surface of the wafer.

Fig. 21

200

LA

IL'

PL'

IF

PB

MA'

MA'

W

P1

P2

BP

MT

PM

WT

PW

M1

C

M2

Y

X